Title: **VLSI Design (EE6805)**
Instructor: **M. Mohiuddin**
Credit Hours: **3**
Pre-requisite: Microelectronics course at undergraduate level. Students are expected to have sound background of MOSFETs, Combinational and sequential circuit design and RC networks.

Aims & Objectives:

The phenomenal and very consistent growth of electronics for the last several decades owes much of its success to the Very Large Scale Integration (VLSI) of the Field Effect Transistors (FETs) which has enabled to reliably pack more than two billion transistors in an Integrated Circuit (IC) chip of area less than 2.5 cm^2. Complementary MOSFET (CMOS), the fundamental building block of almost every digital device on earth, has some very favorable properties like almost zero static power consumption, high noise margin and ease of fabrication that resulted in this revolution of integrated circuits. This course will extensively explore CMOS both from device and circuits' perspective.

With the increased complexity of IC chips, designers tend to spend more time on HDL based specification and rely mainly on EDA tools for the complete design cycle of a chip design. They tend to give less emphasis on the understanding of underlying physics of devices and working of circuits. For new and innovative designs, insight into the physics and detailed working of circuits, and the understanding of the effects of layout and routing must be understood. This course attempts to give an in-depth coverage of MOSFET device, CMOS circuits and their layout, leading to the standard cell based design of combinational and sequential building blocks of a larger VLSI subsystem. Circuit characterization and performance issues are discussed and alternative solutions meeting varied design constraints are explored. By the end of this course, students should have attained the knowledge as per the course contents and be able to:

- Draw layout of basic combinational and sequential building blocks of a larger VLSI design
- Integrate building blocks into a larger VLSI subsystem
- Simulate and do basic functional verification and area/timing optimization of VLSI subsystems
- Suggest alternative CMOS families to meet varied design constraints

Course Contents overview:

1. **Overview of VLSI technology**
   - Introduction to the course and to the VLSI technology, state-of-the-art of VLSI
   - Fundamentals of CMOS, ideal CMOS inverter using static or complementary CMOS logic family and its basic logic gates
   - Introduction to fundamentals of CMOS fabrication process
   - Introduction to layout (layout fundamentals, design rules, stick diagrams, routing and Euler path)

2. **Transistor theory of MOSFETs, parasitics and non-idealities**
   - Overview of MOSFET construction and principle of operation
   - Basic derivation of Ideal I-V characteristics and different regions of operation
   - Capacitance, C-V relationship as a function of bias

- MOSFET non-idealities—channel length modulation, DIBL, Leakage current etc.

3. **CMOS inverter DC analysis**
   - Voltage Transfer Characteristics (VTC).
   - Switching characteristics—rise, fall and propagation time
   - Power dissipation

4. **Circuit Characterization and performance estimation**
   - RC delay models
   - Logical effort and transistor sizing
   - Power dissipation
   - Interconnect

5. **Design of combinational building blocks**
6. **Design of sequential building blocks**
7. **VLSI subsystem design**

Labs:

Labs will primarily be based on the use of Electric (layout editor and SPICE simulator) to design simple gates, building blocks and smaller VLSI sub-systems.

Recommended Books:

1. **Introduction to VLSI circuits and systems by J Uyemura, 2001—**a standard and simpler textbook of VLSI design.
2. **CMOS VLSI Design—A circuits and systems perspective by N Weste et.al. , 4th edition—** Standard, comprehensive and fairly advanced text.

Student Assessment Information Sheet

- **Final exam—40%**
- **Two hourly tests—20%**
- **Term Report and presentation—20% (CMOS limitations in the backdrop of future of miniaturization).**

  You are required to write a report of about 4000 words (15-20 pages including some graphs, pictures, simulation results etc.) and give a presentation on physical limitations of CMOS in the path of continued miniaturization.
  The presentations will be conducted as a student seminar in the presence of GSSE graduate students and faculty members of other research groups as well.

  Assessment strategy:

  1- The report should be written in standard academic US English. Typos and grammatical errors will be harshly penalized.
  2- Thorough understanding of the topic is expected to be reflected by focused literature search, comprehension of any relevant theoretical/technological limitations, prevalent alternative solutions etc.
  3- Discussion and not mere reporting of the results should be given.
  4- Presentation should give brief background and make sense to a graduate student of EE from other research subfields as well.
  5- Report and presentation should be emailed to mohiuddin@pafkiet.edu.pk before 2300 hrs, April 15, 2014.

- **Project—20%**

  Every student is required to work INDIVIDUALLY on one of the following projects:
  - VLSI Design of a simple µprocessor
  - VLSI Design of an FPGA's configurable logic block

  These designs have been thoroughly discussed and partially built in Chapter 3 and Chapter 4 of the book Advanced Cell Design by Sicard (ebook is available in the Project folder).
  - Students are required to fill in the missing bits, migrate the design from Microwind to Electric (major task)
  - Simulate the complete design demonstrating grasp of the working of each building block and of the entire project.
  - Performance estimation including area and speed should be done
  - Project progress will be regularly assessed during labs

  Marks distribution

  - Project progress: 10 marks (to be assessed on the first lab of every month).
  - Final submitted project: 10 marks