FPGA-based Systems Design

This course will introduce FPGA-based system design techniques using VHDL. Introduction to VHDL, advanced hardware design and optimization techniques, and major design examples will be reviewed.

Course Code: EE-6803
Credit Hours: 3 + 0
Pre-requisite: Digital Logic Design, Computer Architecture, Computer Programming

Target Audience: MS/PhD students wishing to pursue research in the field of Embedded Systems, Digital Signal Processing or any other field that may require FPGA based hardware implementation.

Synopsys:
A Field programmable Gate Array (FPGA) is an integrated circuit that is designed to be configured after manufacturing. It combines together the flexibility of microprocessor and high performance of an Application Specific Integrated Circuit (ASIC). FPGAs can be used to implement any logic function that an Application Specific Integrated Circuit (ASIC) can perform. The ease of programming and debugging with FPGAs, as compared to ASICs, decreases the overall non-recurring-engineering (NRE) costs and time-to-market of FPGA-based products. Unlike other technologies, which implement hardware directly into silicon, any errors in the final FPGA-based product can be easily corrected by simply reprogramming the FPGA.

This course will cover two major aspects. (1) VHDL based digital system design. ModelSim will be used to simulate and debug HDL code. (2) Advanced hardware architectural design and optimization techniques. A brief course outline followed in this course is given below.

Brief Course Outline:

From Text Book 1 "RTL Hardware Design Using VHDL, Pong P Chu, 2006"	*From Text Book 2 "Reconfigurable Computing, Scott Hauck, Andre Dehon, 2008"*
1. Introduction to digital system design, VHDL basics and examples, ModelSim based simulation. 2. Quick Overview of synchronous sequential system design including FSM and its basic timing issues. 3. Implementation of FSM based system design using VHDL 4. FSM+D (FSM + Datapath) based system design modeling 5. Pipelining 6. Hierarchical systems and interacting FSM 7. Timing issues of synchronous systems 8. Case studies, examples	9. Implementing applications with FPGA (ch-21) 10. Instance-specific design (ch-22) 11. Precision analysis for Fixed point Computation (ch-23) 12. Distributed Arithmetic (ch-24) 13. Cordic Architectures for FPGA Computing (ch-25) 14. Hardware/Software partitioning (ch-26) 15. SPIHT Image Compression (ch-27) 16. The implications of floating point for FPGAs. (ch-31)

Instructor:
This course will be taught by Dr. Husain Parvez (husain.parvez@pafkiet.edu.pk). He received a PhD degree in Micro Electronics & Computer Science from University Paris-VI, Paris, France. His research interests include design and exploration of FPGA architectures and related CAD tools. He has over three years of industrial experience at the System-on-Chip tools department of Communications Enabling Technologies Islamabad, and at Video Decoder & Optimization department of Streaming Networks Islamabad.

Text Book:
1. *VHDL'06, "RTL Hardware Design Using VHDL – Coding for Efficiency, Portability and Scalability"*. Pong P Chu, 2006
2. RC'08, *"Reconfigurable Computing – The theory and practice of FPGA-based computing"*. Scott Hauck, Andre Dehon, 2008.

Reference Books/Material:
- *EVITA* – Enhanced VHDL Tutorial with Applications.
- *Selected Research Papers*