# Reconfigurable Computing

***A course to introduce internal design of reconfigurable architectures and FPGAs, the CAD tools and algorithms to program these architectures, and application development using these reconfigurable architectures.***

**Course Code**: EE-7805
**Credit Hours:** 3
**Pre-requisite:** Computer Architecture, Data Structures, or instructor's permission
**Target Audience:**
MS/PhD students wishing to pursue research in the field of FPGAs, Reconfigurable Architectures, relevant CAD tools, or application development using FPGAs.

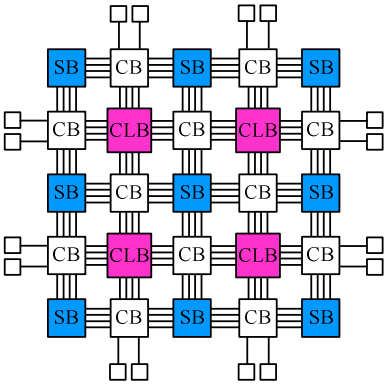
**Synopsis:**

Reconfigurable computers are reprogrammable devices that can be programmed to execute a vast variety of hardware circuits. A software CAD flow transforms a hardware circuit to a programming bitstream, which can be easily and instantly programmed on the reconfigurable device. Consequently, hardware circuits mapped on these architectures have less NRE cost and shorter time-to-market as compared to alternate technologies that fabricate application circuits on silicon. Any errors or updates in the final product can also be easily upgraded.

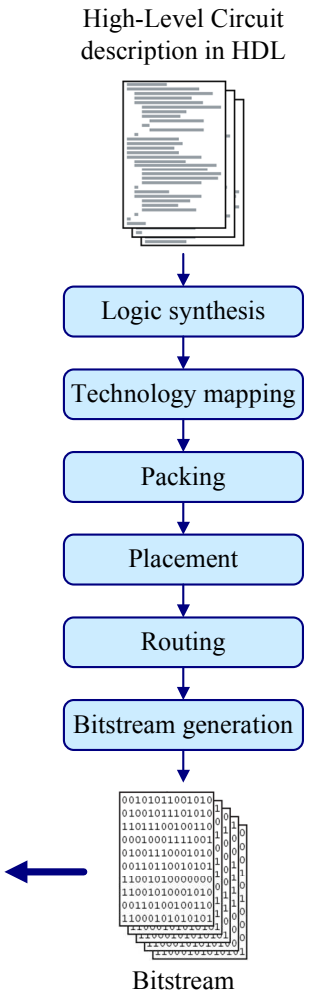
This course will review the state-of-the-art in reconfigurable computing, both from the hardware as well as the software aspect. Hardware aspect will primarily cover the internal architecture of Field Programmable Gate Arrays (FPGA), a widely used reconfigurable device, and many other reconfigurable systems. The Configurable Logic Blocks (CLBs), customized hard logic blocks, configurable routing network, hardware organization etc. will be examined to get a flavor of the hardware limitations of these reprogrammable devices.

Software aspect will primarily review the computer-aided-design (CAD) tools and the algorithms required to program hardware application circuits on these reconfigurable devices. The issues of placement (selection of circuit component's location on the architecture) and routing (circuit interconnection of components using reconfigurable routing network) will be thoroughly reviewed.

Performance of FPGAs will later be compared with ASICs, microprocessors and different other digital platforms. Existing reconfigurable systems will be examined to identify their limitation and to highlight directions for future research.



Abstract view of island-style FPGA



A typical FPGA mapping flow

**Instructor:**

Husain Parvez received his Bachelors of Engineering in Computer Science from National University of Sciences and Technology, Rawalpindi. He has over three years of work experience at the System-on-Chip tools department of Communications Enabling Technologies Islamabad, and at Video Decoder & Optimization department of Streaming Networks Islamabad. He received MS and PhD in Micro-electronics from University Paris-VI, Paris, France. His current research interests include design and exploration of FPGA architectures and related CAD tools.

**Course Outline:**

- FPGA architecture, basic blocks, routing network, etc.
- FPGA mapping flow, placement/routing algorithms, etc.
- Application development for FPGA
- Contrasting ASIC, FPGA, microprocessors,
- Reconfigurable systems, Reconfigurable processors
- High level compilation – C to FPGA
- Current trends and direction for future research

**Recommended Books:**

1. Scott Hauck, Andre Dehon. *Reconfigurable Computing – The theory and practice of FPGA-based computing – 2008*.
2. Christophe Bobda. *Introduction to Reconfigurable Computing – Architecture, algorithms and applications – 2007*.
3. Vaughn Betz, Jonathan Rose, Alexander Marquardt. *Architecture and CAD For Deep-Submicron FPGAs – 1999.*