FPGA-based Systems Design

This course will introduce FPGA-based system design techniques using VHDL. Advanced hardware optimization techniques, and some major design examples will also be reviewed.

Course Code: EE-6803
Credit Hours: 3 + 0
Pre-requisite: Digital Logic Design, Computer Architecture, Computer Programming

Target Audience: MS/PhD students wishing to pursue research in the field of Embedded Systems, Digital Signal Processing or any other field that may require FPGA based hardware implementation.

Synopsys:
A Field programmable Gate Array (FPGA) is an integrated circuit that is designed to be configured after manufacturing. It combines together the flexibility of microprocessor and high performance of an Application Specific Integrated Circuit (ASIC). FPGAs can be used to implement any logic function that an Application Specific Integrated Circuit (ASIC) can perform. The ease of programming and debugging with FPGAs, as compared to ASICs, decreases the overall non-recurring-engineering (NRE) costs and time-to-market of FPGA-based products. Unlike other technologies, which implement hardware directly into silicon, any errors in the final FPGA-based product can be easily corrected by simply reprogramming the FPGA.

This course will cover two major aspects. (1) VHDL: One of the widely used hardware description language. (2) Advanced hardware architectural design and optimization techniques. A brief course outline followed in this course is given below.

Brief Course Outline:

From Text Book 1 "RTL Hardware Design Using VHDL, Pong P Chu, 2006"	*From Text Book 2 "Reconfigurable Computing, Scott Hauck, Andre Dehon, 2008"*
1. Overview of FPGA architecture, software flow, FPGA vs ASIC. Overview of ModelSim. 2. Basic language constructs of VHDL (ch-3,4,5) • Concurrent signal assignment statements • Sequential signal assignment statements 3. Operator sharing/ Functionality sharing (ch-7) 4. Design examples (ch-7,8) • Combinational circuit design examples • Sequential circuit design examples 5. Finite State Machines (ch-10) 6. Register Transfer methodology (ch-11) 7. Pipelining (ch-9) 8. Hierarchical Design in VHDL (ch-13) 9. Timing analysis (ch-6,8,10)	10. Implementing applications with FPGA (ch-21) 11. Instance-specific design (ch-22) 12. Precision analysis for Fixed point Computation (ch-23) 13. Distributed Arithmetic (ch-24) 14. Cordic Architectures for FPGA Computing (ch-25) 15. Hardware/Software partitioning (ch-26) 16. Multi-FPGA Systems : Logic Emulation (ch-30) 17. The implications of floating point for FPGAs. (ch-31) 18. Summary of latest research trends regarding FPGA-based Systems and Reconfigurable Computing.

Instructor:
This course will be taught by Dr. Husain Parvez (husain.parvez@pafkiet.edu.pk). He received a PhD degree in Micro Electronics & Computer Science from University Paris-VI, Paris, France. His research interests include design and exploration of FPGA architectures and related CAD tools. He has over three years of industrial experience at the System-on-Chip tools department of Communications Enabling Technologies Islamabad, and at Video Decoder & Optimization department of Streaming Networks Islamabad.

Text Book/Reference Material:
1. *"RTL Hardware Design Using VHDL – Coding for Efficiency, Portability and Scalability"*. Pong P Chu, 2006
2. *"Reconfigurable Computing – The theory and practice of FPGA-based computing"*. Scott Hauck, Andre Dehon, 2008.
3. *Selected Research Papers*

Marks Distribution:

Final	Hourly	Assignment	Literature review report	Total
40%	20%	30%	10%	100%