Reconfigurable Computing

A course to introduce internal design of reconfigurable architectures and FPGAs, the CAD tools and algorithms to program these architectures, and application development using these reconfigurable architectures.

Course Code: EE-7805
Credit Hours: 3
Pre-requisite: Computer Architecture, Data Structures, or instructor's permission
Target Audience:
MS/PhD students wishing to pursue research in the field of FPGAs, Reconfigurable Architectures, relevant CAD tools, or application development using FPGAs.

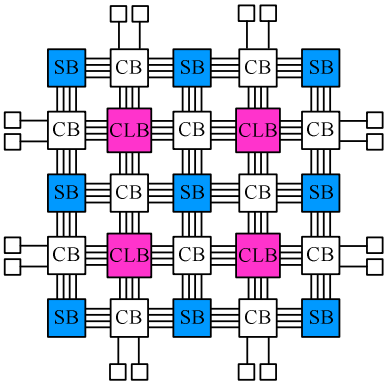
Synopsis:

Reconfigurable computers are reprogrammable devices that can be programmed to execute a vast variety of hardware circuits. A software CAD flow transforms a hardware circuit to a programming bitstream, which can be easily and instantly programmed on the reconfigurable device. Consequently, hardware circuits mapped on these architectures have less NRE cost and shorter time-to-market as compared to alternate technologies that fabricate application circuits on silicon. Any errors or updates in the final product can also be easily upgraded.

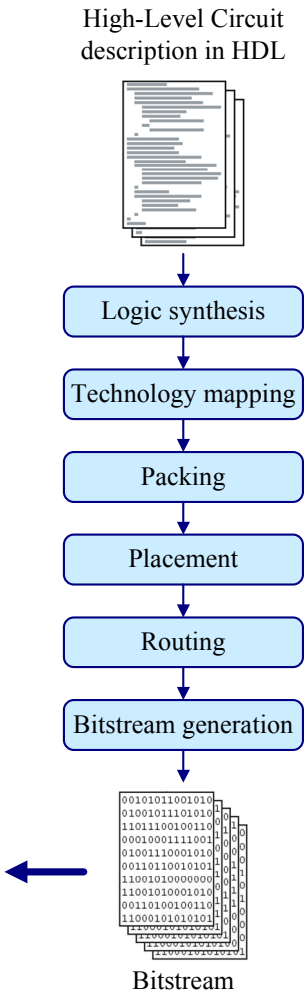
This course will review the state-of-the-art in reconfigurable computing, both from the hardware as well as the software aspect. Hardware aspect will primarily cover the internal architecture of Field Programmable Gate Arrays (FPGA), a widely used reconfigurable device, and many other reconfigurable systems. The Configurable Logic Blocks (CLBs), customized hard logic blocks, configurable routing network, hardware organization etc. will be examined to get a flavor of the hardware limitations of these reprogrammable devices.

Software aspect will primarily review the computer-aided-design (CAD) tools and the algorithms required to program hardware application circuits on these reconfigurable devices. The issues of placement (selection of circuit component's location on the architecture) and routing (circuit interconnection of components using reconfigurable routing network) will be thoroughly reviewed.

Performance of FPGAs will later be compared with ASICs, microprocessors and different other digital platforms. Existing reconfigurable systems will be examined to identify their limitation and to highlight directions for future research.



Abstract view of island-style FPGA



A typical FPGA mapping flow

Instructor:
Husain Parvez received his Bachelors of Engineering in Computer Science from National University of Sciences and Technology, Rawalpindi. He has over three years of work experience at the System-on-Chip tools department of Communications Enabling Technologies Islamabad, and at Video Decoder & Optimization department of Streaming Networks Islamabad. He received MS and PhD in Micro-electronics from University Paris-VI, Paris, France. His current research interests include design and exploration of FPGA architectures and related CAD tools.

Course Outline:
- FPGA architecture, basic blocks, routing network, etc.
- FPGA mapping flow, placement/routing algorithms, etc.
- Application development for FPGA
- Contrasting ASIC, FPGA, microprocessors,
- Reconfigurable systems, Reconfigurable processors
- High level compilation – C to FPGA
- Current trends and direction for future research

Recommended Books:
1. Scott Hauck, Andre Dehon. *Reconfigurable Computing – The theory and practice of FPGA-based computing – 2008.*
2. Christophe Bobda. *Introduction to Reconfigurable Computing – Architecture, algorithms and applications – 2007.*
3. Vaughn Betz, Jonathan Rose, Alexander Marquardt. *Architecture and CAD For Deep-Submicron FPGAs – 1999.*

Marks distribution:

Final	50 %
Mid-term	25 %
Project + Presentation	15 %
Assignments + Quizzes	10 %

Project

Write HDL code for a 5x5 mesh-based FPGA architecture with uni-directional single driver routing network having channel width=4. Test your FPGA architecture on ModelSim by programming a small test application e.g. 4-adder application. The bitstream of the test application must be generated by using academic CAD tool modules.

Detailed Course Outline

Tentative course outline is given below

Week	Details
1. 2.	**Introduction** – Why Reconfigurable Computing - Introduction? List of conferences, journals, people and companies working in the domain of reconfigurable computing. Different major areas of reconfigurable computing (architecture, tools, applications, device technology). Miscellaneous announcements (Summary of the entire course outline, Grading System, Google Drive) **Hardware Device technologies** – Digital revolution, advent of transistors, Full-custom ASIC, Standard-cell ASIC, Gate-array ASIC, Complex field programmable devices, Simple field programmable devices, SSI/MSI components. **Architecture and use of a LUT** – Boolean equations, Truth tables, A simple 3-input LookUp-Table (LUT), example of mapping a boolean equation on a LUT, mapping different literal to a different input. **Detailed internal architecture of an academic mesh-based FPGA –** Basic Logic element (BLE), Configurable Logic Block (CLB), mesh-based bi-directional routing network, switch box, connection box, Fc-in, Fc-out, I/Os, in-rate and out-rate, long wires, mesh-based uni-directional routing network and single driver wires, Fs, different topologies of a switch box. **Overview of software flow** – HDL, Synthesizer, boolean equations and flip-flops, Technology mapping, LUTs and flip-flops, Packing, CLBs, Placement, Routing, Bitstream generation. **Heterogeneous FPGA architecture** – Hard-logic blocks such as DSP blocks, Multipliers, RAMs, Hard processor blocks, or soft-core processors, shadow cluster. **Tree-based hierarchical FPGA architecture -** **Tile-based layout of FPGA architectures** – **ASIC vs FPGA vs Microprocessor** – **Architecture exploration** – Data-structures, area model, timing model **Reading Assignment:** "FPGA Architecture: Survey and Challenges", Foundations and Trends in Electronic Design Automation Vol. 2, No. 2 (2007) 135–253, 2008 I. Kuon, R. Tessier and J. Rose
3.	**Project discussion, details** Develop a 5x5 FPGA architecture in VHDL. Simulate on ModelSim
4.	**Simulated annealing-based placement algorithm –** Introduction to placement algorithms, detailed algorithm analysis of simulated annealing-based placement algorithm, other placement algorithms.

	Reading Assignment: "Directional and Single-Driver Wires in FPGA Interconnect", Guy Lemieux, Edmund Lee, Marvin Tom and Anthony Yu, ICFPT 2004.
5.	**Path-finder routing algorithm –** Introduction to routing algorithm, detailed algorithm analysis of path finder routing algorithm. **Reading Assignment:** "HARP: Hard-wired Routing Pattern FPGAs", Satish Sivaswamy, Kia Bazargan, Gang Wang, Ryan Kastner, Cristinel Ababei and Eli Bozorgzadeh, FPGA 2005
6.	**Commercial FPGA architectures –** Xilinx, Altera, HardCopy, EasyPath, eASIC, Tabula **Reading Assignment:** "Tabula's Time Machine Rapidly Reconfigurable Chips Will Challenge Conventional FPGAs"
7.	**Reconfigurable Computing Architectures:** Chapter-2 RC book **Reading/Listening Assignment:** "FPGAs in 2032 video lectures" (http://tcfpga.org/fpga2012/)
8.	**Reconfigurable Computing Systems:** Chapter-3 RC book
9.	**Technology mapping –** Introduction, detailed algorithm **Multi-FPGA systems :** Chapter 30 RC book
10.	**Hardware/software partitioning:** Chapter 26 RC book **Compiling C for spatial computing :** Chapter 7 RC book
11.	**OS support for Reconfigurable computing:** Chapter 11 RC book
12.	**Reconfiguration Management:** Chapter 4 RC book
13.	**Fast Compilation Techniques:** Chapter 20 RC book **Reading/Listening Assignment:** "Hardware assisted Simulated Annealing with application for fast FPGA Placement",
14. 15.	**Selected research papers –** Two or three current research papers
16.	**Revision + extra class to complete contents + project discussion**

Reading/Listening Assignment #5: "FPGAs in 2032 video lectures" (http://tcfpga.org/fpga2012/)
Discussion/Quiz on Assignment #5

Reading Assignment #6: Michael G. Wrighton, Adre Dehon, ACM FPGA, 2003
Discussion/Quiz on Assignment #6.