Advanced Computer Architecture – Fall 2018

Tentative Course Outline

1.	Week 1	Introduction: Fundamentals of Computer Design, Introduction, RISC vs CISC, Instruction Set Architecture
2.	Week 2,3,4,5	Pipelining: Basic and Intermediate Concepts, Pipeline hazards (Structural, Control and Data), Solution to Pipeline hazards (Forwarding, Interlocks, Code Reordering, branch prediction), Introduction to VHDL, Single Cycle MIPS Data path and Control Path implementation using VHDL, Pipelined MIPS hardware implementation using VHDL
3.	Week 6,7	Memory Hierarchy Design, Cache design, Virtual memory design, Compiler optimization to exploit cache
4.	Week 8,9	VLIW and Super-scalar architectures. Detailed internal architecture of VLIW processor, detailed internal architecture of Super-scaler architecture. Compiler optimization to exploit VLIW processor (Instruction scheduling, Loop unrolling, Software pipelining, register renaming, etc)
5.	Week 10	Vector Processors
6.	Week 11	Data Level Parallelism in Vector, SIMD and GPU architectures
7.	Week 12	Thread-Level Parallelism, Students Presentation
8.	Week 13	Ware house scale Computers, Computer Architecture, Memory, Cloud Computing, Student Presentations
9.	Week 14	Domain Specific Architectures, Deep Neural Networks, Google's Tensor Processing Unit, Microsoft Catapult, Intel Crest, Pixel Visual Core
10.	Week 15	Latest research trends in Computer Architecture, Student Presentations

About Instructor:

Husain Parvez received his Bachelors of Engineering in Computer Science from National University of Sciences and Technology, Rawalpindi. He received MS and PhD in Electronics and Computer Science from University Pierre & Marie Curie (Paris-6), Paris. Before doing MS and PhD, he worked at the System-on-Chip tools department at Communications Enabling Technologies Islamabad, and at Video Decoder & Optimization department at Streaming Networks Islamabad. He is associated with PAF-KIET since 2012. His current research interests include design and exploration of FPGA architectures and related CAD tools for FPGAs.

Dr. Parvez was the co-principal investigator of two ICTR&D funded projects, each worth 14 million rupees. He has also worked on funded projects of mutual interest in collaboration with international partners. He has authored and co-authored 7 publications in high impact journals, and 15 papers in international conferences. He has also authored a book titled "Application-Specific Mesh-based Heterogeneous FPGA Architectures" published by Springer.

Project

Write, test and simulate a pipelined MIPS processor using VHDL/Verilog or Protieus

Text book:

"Computer Architecture – A quantitative approach", John L Hennessy, David A Patterson, Sixth Edition.

Marks Distribution

Final	50
Mid term	20
Project(s)	15
Presentation	10
Quiz + Assignment	05
Total	**100**